[ON-CHIP ESD PROTECTION CIRCUIT WITH A SUBSTRATE-TRIGGERED SCR DEVICE]

Abstract of Disclosure

An ESD (electrostatic discharge) protection circuit is electrically connected to an I/O buffering pad, an internal circuit (IC), a V_{SS} power terminal and a V_{DD} power terminal. The ESD protection circuit comprises a first ESD-detection circuit electrically connected between the I/O pad and the V_{SS} power terminal, a second ESD-detection circuit electrically connected between the I/O pad and the V_{DD} power terminal, a P-STSCR comprising a first lateral SCR and a P trigger node, and an N-STSCR comprising a second lateral SCR and an N trigger node. When a positive-to-V_{SS} ESD event occurs on the I/O buffering pad, the first ESD-detection circuit generates a first trigger current to the P-trigger node of the P-STSCR to trigger the first lateral SCR. The P-STSCR is thus quickly turned on, and current incurred from the positive voltage pulse is discharged to the V_{SS} power terminal. When a negative-to-V_{DD} ESD event occurs on the I/O buffering pad, the second ESD-detection circuit generates a second trigger current to the N-trigger node of the N-STSCR to trigger the second lateral SCR. The N-STSCR is quickly turned on, and current incurred from the negative voltage pulse is discharged to the V_{DD} power terminal. In contrast to the prior method of making an on-chip ESD protection circuit, the present invention uses a substrate-triggered SCR device with a much lower switching voltage in the protection circuit, and applies the protection circuit to input ESD protection circuits, output ESD protection circuits, and power-rail ESD clamp circuits. ESD robustness of the IC product in the deep submicron CMOS processes is improved, and the total layout area of the on-chip ESD protection circuit is reduced.

Figures